Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the non-compliance.

Amended claim 15 now positively defines the external register present lead to be separate from the test data input lead and the test data output lead, in addition to being connected to the instruction register and extending beyond the periphery of the functional IP core circuits.

In contrast, US 6,173,428 to West teaches that the TAP controller 32 is a finite-state machine having a state transition diagram as shown in FIG. 3. The TAP controller 32 controls the several operating modes for testing the device logic 22, testing the external input pin 24 and output pin 26 connections, and for controlling any other operations utilizing the user-defined registers 40 in boundary scan test. The TAP controller 32 has 16 states.

Figure 5 depicts an output lead extending from finite-state machine TAP controller logic 32 that is labeled "ENABLE FOR USER DEF. REGISTERS". No shift register is disclosed in finite-state machine TAP controller logic 32. A search of the text reveals that the specification provides no further description of this specific lead. The specification only states that the TAP controller controls "any other operations utilizing the user-defined registers 40 in boundary scan test".

User-defined registers 40 are not external registers. They are internal to the boundary scan test logic 30. See Figure 4.

None of the figures in the West patent depict and the text does not describe a lead comparable to the claimed external register present lead separate from the test data input and output leads, connected to the instruction register, and extending beyond the periphery of the functional IP core circuits.

The Action says that "West shows that the TAP controller shifts in the mode selection signals including the external register enable signal "labeled as 'user def. registers' in fig. 5: the logical state of the external register present signal are examined in order to determine the mode of operation of the boundary scan system".

This statement in the Action fails to address the presently claimed limitations of the external register present lead being separate from the test data input lead and the test data output lead, being connected to the instruction register and extending beyond the periphery of the functional IP core circuits.

Claim 15 is patentable.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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